WHAT IS CLAIMED IS:

1. A prefetch controller for controlling retrieval of data from a data storage device in response to a current host command received from a host device, the prefetch controller comprising:

a sequential read detector configured to generate a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential; and

a transfer length generator configured to provide a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, and provide a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command.

2. The prefetch controller of claim 1, wherein the first transfer length value is larger than the second transfer length value.

3. The prefetch controller of claim 1, wherein the sequential read detector comprises:

operation compare logic configured to compare an operation specified in the current host command to an operation specified in the previously received host command, and generate a first indication for the current host command if the compared operations are both read operations.

4. The prefetch controller of claim 3, wherein the sequential read detector further comprises:

address compare logic configured to compare a first address associated with the current host command to a second address associated with the previously received host command, and generate a second indication for the

current host command if the compared addresses are indicative of sequential operations.

5. The prefetch controller of claim 4, wherein the sequential read detector further comprises:

a sequential read indication generator configured to generate the new sequential read indication if the first and the second indications are not generated for the current host command.

6. The prefetch controller of claim 1, wherein the sequential read detector comprises:

a plurality of registers for storing an opcode specified in the current host command, an opcode specified in the previous host command, a start address associated with the current host command, and an end address associated with the previous host command.

7. The prefetch controller of claim 6, wherein the sequential read detector further comprises:

opcode compare logic for comparing the stored opcodes;

address increment logic for incrementing the stored end address, thereby generating an incremented end address; and

address compare logic for comparing the stored start address and the incremented end address.

8. The prefetch controller of claim 7, wherein the sequential read detector further comprises:

a sequential read indication generator configured to generate the new sequential read indication based on outputs of the opcode compare logic and the address compare logic.

9. The prefetch controller of claim 1, wherein the transfer length generator comprises:

a first register for storing a prefetch value;

a second register for storing a zero value; and

a multiplexer coupled to the first and the second registers, the multiplexer responsive to the new sequential read indication for selectively outputting the prefetch value or the zero value.

10. The prefetch controller of claim 9, wherein the transfer length generator further comprises:

a third register for storing a transfer length value specified in the current host command.

11. The prefetch controller of claim 10, wherein the transfer length generator further comprises:

an adder for adding the value stored in the third register and the value output by the multiplexer.

12. A method of transferring data between a host electronic device and a data storage device, the method comprising:

receiving a current read command from the host electronic device, the current read command specifying a first transfer length value;

identifying whether the current read command is non-sequential to a previously received read command;

adding a prefetch length value to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value; and

outputting the second transfer length value to the data storage device.

13. The method of claim 12, and further comprising:

buffering a first set of data received from the data storage device, the first set of data corresponding to the first transfer length value; and

outputting the buffered first set of data to the host electronic device.

14. The method of claim 13, and further comprising:

buffering a second set of data received from the data storage device, the second set of data corresponding to the prefetch length value; and

outputting the buffered second set of data to the host electronic device in response to a subsequently received sequential read command.

15. The method of claim 12, wherein the step of identifying whether the current read command is non-sequential comprises:

comparing opcodes specified in commands received from the host electronic device; and

comparing address information associated with the commands received from the host electronic device.

16. The method of claim 12, and further comprising:

adding a zero value to the first transfer length value if the current read command and the previous read command are sequential, thereby generating the second transfer length value.

17. A memory device comprising:

storage means for storing data;

host interface means for receiving host commands from a host electronic device;

sequential read detection means for identifying whether a current host command specifies a non-sequential read operation; and

transfer length generation means for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation, the transfer length

generation means configured to output a sum of the prefetch length value and the transfer length value to the storage means.

18. The memory device of claim 17, wherein the sequential read detection means comprises:

means for comparing an operation specified in the current host command to an operation specified in a previously received host command; and

means for comparing a first address associated with the current host command to a second address associated with the previously received host command.

19. The memory device of claim 17, wherein the transfer length generation means comprises:

first register means for storing the prefetch length value;

second register means for storing a zero value;

multiplexing means for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection means; and

adding means for adding an output of the multiplexing means and the transfer length value specified in the current host command.

20. A computer-readable medium having computer-executable instructions for performing a method of transferring data between a host electronic device and a data storage device, the method comprising:

receiving a current host command from the host electronic device;

generating a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential;

outputting a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command; and

outputting a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command, the second transfer length value less than the first transfer length value.

21. The computer-readable medium of claim 20, wherein the first transfer length value is larger than the second transfer length value.

22. The computer-readable medium of claim 20, wherein the method further comprises:

comparing an operation specified in the current host command to an operation specified in the previously received host command; and

generating a first indication for the current host command if the compared operations are both read operations.

23. The computer-readable medium of claim 22, wherein the method further comprises:

comparing a first address associated with the current host command to a second address associated with the previously received host command; and

generating a second indication for the current host command if the compared addresses are indicative of sequential operations.

24. The computer-readable medium of claim 23, wherein the new sequential read indication is generated only if the first and the second indications are not generated for the current host command.

25. The computer-readable medium of claim 20, wherein the method further comprises:

storing an opcode specified in the current host command, an opcode specified in the previous host command, a start address associated with the current host command, and an end address associated with the previous host command.

26. The computer-readable medium of claim 25, wherein the method further comprises:

comparing the stored opcodes;

incrementing the stored end address, thereby generating an incremented end address; and

comparing the stored start address and the incremented end address.

27. The computer-readable medium of claim 26, wherein the new sequential read indication is generated based on results of the opcode comparisons and the address comparisons.

28. The computer-readable medium of claim 20, wherein the method further comprises:

storing a prefetch value;

storing a zero value; and

selectively outputting the prefetch value or the zero value based on whether the new sequential read indication is generated for the current host command.

29. The computer-readable medium of claim 28, wherein the method further comprises:

storing a transfer length value specified in the current host command.

30. The computer-readable medium of claim 29, wherein the method further comprises:

adding the stored transfer length value and the selectively output value.